CARIOCA - A Fast Binary Front-End Implemented in 0.25μm CMOS using a Novel Current-Mode Technique for the LHCb Muon Detector

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Abstract

The CARIOCA front-end is an amplifier discriminator chip, using 0.25μm CMOS technology, developed with a very fast and low noise preamplifier. This prototype was designed to have input impedance below 10Ω. Measurements showed a peaking time of 14ns and noise of 450e^- at zero input capacitance, with a noise slope of 37.4 e^-/pF. The sensitivity of 8mV/fC remains almost unchanged up to a detector capacitance of 120pF.

I. INTRODUCTION

The investigation of the characteristics of state-of-the-art deep submicron CMOS technologies show that analogue circuits with very good performance can be designed using these processes. In particular, deep submicron technologies are well suited for the design of binary front-end systems. In these applications, the limitation on the dynamic range imposed by the squeezed power supplies is not the primary issue [1-3].

Current-mode architectures are an attractive alternative to the more conventional voltage-mode ones for very fast circuits. In the current mode approach, the signal is processed in the current domain, thus avoiding charging and discharging of the parasitic capacitance to "high" voltage levels and keeping the internal nodes of the circuit at low impedance values. Therefore, combining current-mode techniques with the use of deep submicron technologies provides the opportunity of building analog circuits with high speed and low power consumption.

The front-end CARIOCA has been designed in two versions: one optimised for the readout of the Multi Wire Proportional Chambers (MWPC) of the LHCb Muon system [4] and the other for silicon strip detectors. This paper presents only the requirements and results for the LHCb muon chambers, which is the more challenging in terms of detector capacitance up to 200pF. This work has been done in the framework of the CERN RD49 project [5].

II. FRONT - END REQUIREMENTS

The LHCb Muon System [6] is composed of five muon detector stations, which provide muon identification and Level-0 muon trigger formation. Each station is required to have an efficiency above 99% within a 20ns time window. This translates into a time resolution of 3.5ns (rms) for the double gap MWPCs with a wire spacing of 1.5mm.

The total number of MWPC is approximately 600, which corresponds to 125K readout channels. High rates of up to 800KHz per channel in some detector regions require optimised tail cancellation and baseline restoration circuits. The maximum integrated dose in the Muon system is of 1Mrad requiring radiation hard technology.

The capacitances of the MWPCs range from about 10pF to 200pF. This capacitance together with the preamplifier input resistance define a time constant, $\tau_{in} = R_{in} \cdot C_{in}$, that ultimately limits the front-end speed. In addition, an amplifier input resistance below 50Ω is required in order to limit the capacitive crosstalk.

A good time resolution at a gas gain of about $2 \cdot 10^5$ requires a very low threshold combined with high speed and low noise front-end for detector capacitances up to 200pF. Calculations [7] show that a peaking time of about 10ns is a good compromise in terms of time resolution and stability of the signal discrimination.

III. CIRCUIT DESCRIPTION

Fast low noise pulse amplifiers are usually based on charge or transimpedance circuits, and have limited performance at large detector capacitance. This limitation is due to the fact that the feedback network, which converts the output voltage into an input current, must have low impedance in order to keep the closed loop gain small enough to get a high speed response. As a consequence, the charge-to-voltage gain is smaller and the noise performance reduced. The present front-end uses a novel low noise current mode feedback circuit that can amplify current signals of large detector capacitances at very high speed without having significantly more noise than a charge amplifier.

The prototype, shown in Figure 1, is a eight-channel low noise amplifier discriminator binary front-end developed in a 0.25μm CMOS technology, operating at 2.5V. The present version of the CARIOCA front-end has been optimised for detector capacitances up to 120pF.

Each processing channel is formed by a current mode preamplifier, a three-stage discriminator and a LVDS driver. The overall chain is DC, allowing very high counting rate readout operation without baseline shift effects. Only one signal return path is used (ground) to be

more robust on power supply rejection. Each channel has an independent biasing and threshold circuit, which may avoid crosstalk between channels. The analog structure of a single channel is shown in Figure 2. The detailed circuit schematic is described in [8].

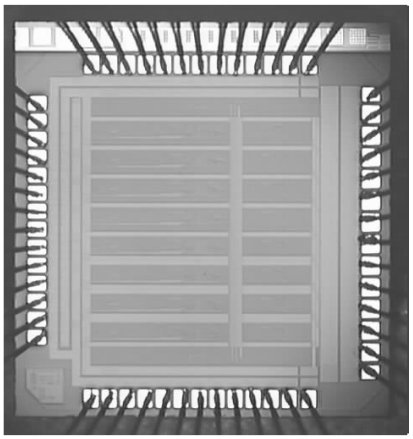

Figure 1: Photo of the 2x2mm^2 prototype with eight channels.

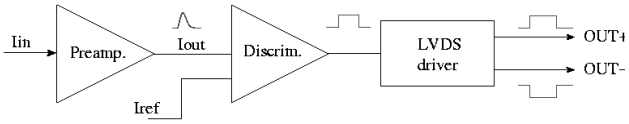

Figure 2: CARIOCA block diagram.

A. *Preamplifier*

The preamplifier, shown in Figure 3, is a n-channel structure with an active feedback and a large input transistor with W/L of 1600µm/0.7µm. The drain current of 2mA is determined by a p-channel cascode current source, with independent networks for the bias voltages. A current mirror follows the first stage of amplification. The transconductance ratio of the transistors $N3$ and $N4$ gives the preamplifier current gain

$$\frac{I_{OUT}}{I_{IN}} = \frac{g_{m_{N4}}}{g_{m_{N3}}} .$$

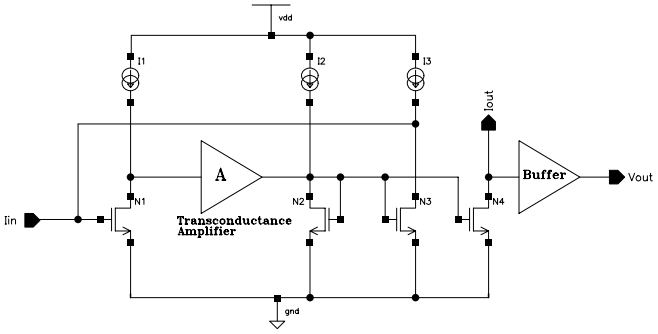

Figure 3: Simplified preamplifier schematic.

Due to the feedback, the input impedance is determined by

$$R_{IN} = \left(g_{m_{N1}} g_{m_{N2}} g_{m_{N3}} R_{N1} R_{N2}\right)^{-1} ,$$

where R_{N1} and R_{N2} are the resistances on the drain nodes of the transistors $N1$ and $N2$. For medium frequencies the input resistance stays at about 10Ω.

B. *Discriminator*

The discriminator consists of 3 stages: a current discriminator, a voltage sensing amplifier and a buffer followed by a LVDS driver, as shown in Figure 4. A baseline restoration based on a DC servo loop (not shown) ensures both dynamic stability of the baseline and offset cancellation necessary with the fully DC coupled circuit.

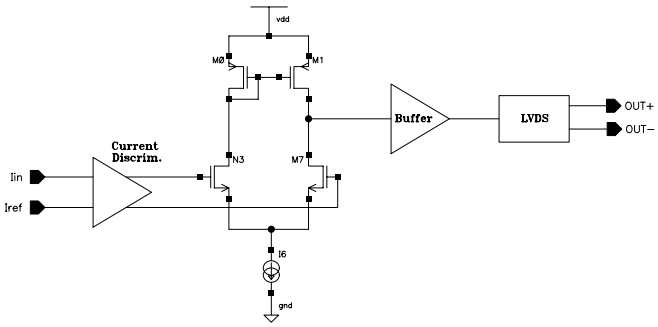

Figure 4: Discriminator block diagram.

IV. MEASUREMENT RESULTS

Measurements have been done for the CARIOCA low gain version, optimised for an input capacitance of 120pF. Examples of analog and digital signals are shown in Figure 5 and 6, at an input capacitance of 15pF. The positive overshoot is due to the baseline restoration circuit that produces a bipolar shape.

It is important to notice that all measurements were performed using delta input with a rise time of 5ns that may reduce the preamplifier speed and sensitivity.

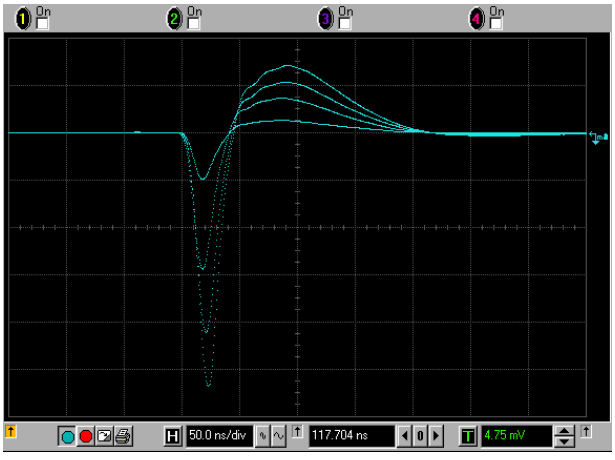

Figure 5: CARIOCA analog output signals for input pulses from 10fC to 40fC, at an input capacitance of about 15pF.

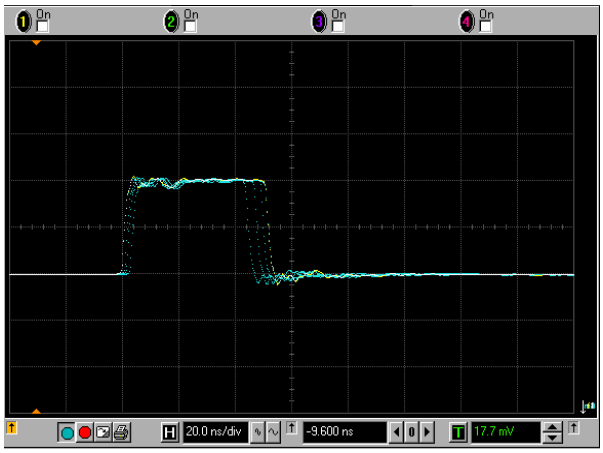

Figure 6: CARIOCA digital output signals for input pulses from 60fC to 100fC, at an input capacitance of about 15pF.

A. *Peaking time*

Figure 7 shows the peaking time versus the detector capacitance. The measurement shows a peaking time of 14ns at C_{det}=0pF and a weak dependence with the input capacitance. The discrepancy with relation to the simulation is of about 15%. If a delta input of 1ns rise time is considered, a 2ns reduction on the peaking time can be obtained.

The expected peaking time for the preamplifier alone is about 8ns. The deterioration of the preamplifier speed is due to the increase of capacitance in the coupling with the discriminator stage.

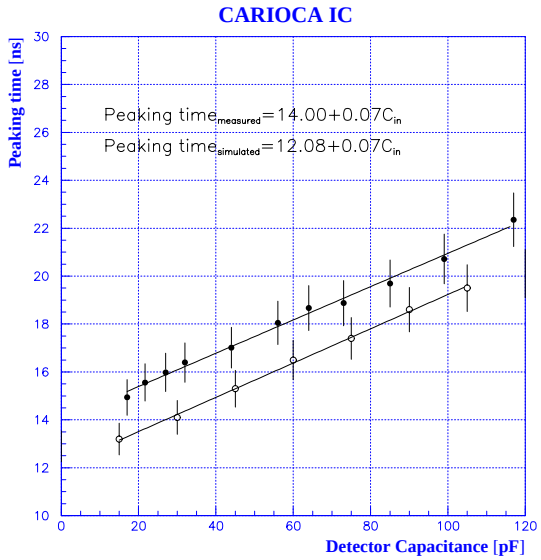

Figure 7: Preamplifier peaking time versus the input capacitance for measurement (closed circle) and simulation (open circle).

B. *Sensitivity*

The sensitivity, shown in Figure 8, was measured for different detector capacitances and showed good uniformity up to 120pF within 5% error. The preamplifier gain is about 8mV/fC using a delta input, as mentioned before. Good agreement between the simulation and the measurement was found.

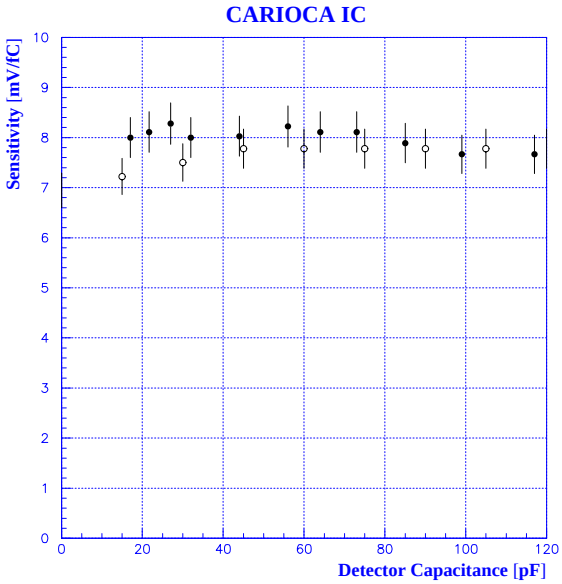

Figure 8: Preamplifier sensitivity as a function of the input capacitance. The measurements are shown as closed circle and simulation as open circle.

C. *Noise versus Detector Capacitance*

The noise measurements were performed with a drain current of 2mA at the input transistor and a peaking time of 14ns. The results are show in Figure 9 together with the calculations. A parallel noise of 450e$^-$ was measured. The noise slope is about 37.4e$^-$/pF for input capacitance up to 50pF and 54.4e$^-$/pF for higher capacitances. The noise slope difference for low and high capacitance values is not fully understood. A brief calculation has shown a parallel noise of 416e$^-$ with a noise slope of 35.9e$^-$/pF and an equivalent input noise voltage of 0.7nV/√Hz. The flicker noise was estimated to be 1.2e$^-$/pF. The noise calculation was performed considering a weighting function with a bipolar shape, as described in [9], and resulted in the following equations for the parallel, serial and flicker noise, respectively:

$$ENC_p^2 = \frac{4KT}{R_p} \cdot t_{peak}$$

$$ENC_s^2 = \frac{4KTn\gamma}{g_m t_{peak}} \cdot C_{in}^2$$

$$ENC_{1/f}^2 = A_f \cdot C_{in}^2$$

K is the Boltzman constant, T the absolute temperature, t_{peak} the signal peaking time and C_{in} the input capacitance. The parallel input resistance R_p is about 50KΩ and the gate transconductance of the input transistor g_m is 30mS. The noise characteristics of 0.25µm CMOS technology [10], n, γ and A_f , were estimated to be 1.4, 0.6 and 4.10^{-14} V^2/Hz, respectively.

For RC-CR filters of 25ns, normally used in several LHC front-end circuits, the noise slope is approximately 27e^-/pF for low input capacitances and 40.7e^-/pF for high capacitances.

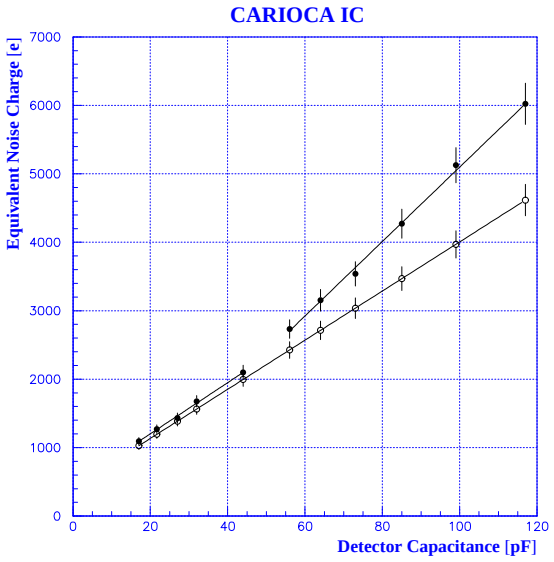

Figure 9: Equivalent Noise Charge measured (closed circle) and calculated (open circle) as a function of the detector capacitance for a peaking time of 14ns. The slope obtained for low capacitance is 37.4e^-/pF and for high capacitance 54.4e^-/pF. Calculations showed a noise slope of 35.9e^-/pF.

The total power consumption was measured to be 12mW per channel, including the discriminator and LVDS driver.

The irradiation tests are not done yet, but previous results using 0.25µm CMOS technologies combined with enclosed layout transistors and guard-rings have shown a very good resistance to total dose radiation damage up to 30MRad [11].

V. Conclusions and Future Plans

An eight-channel amplifier has been produced using 0.25µm CMOS technology. The tests of the four low gain channels, optimised for 120pF of input capacitance, have shown excellent agreement with the expected results from simulations.

Noise measurements indicate an excellent performance of the current mode feedback and agree with noise calculations based on the models for 0.25µm CMOS technology.

A new prototype with 14-channels of each low and high gain version will be produced to study channel uniformity and crosstalk. A 16-channel amplifier with shaper and baseline restoration circuits is under development. The final goal is a circuit for both anode and cathode readout, optimised for an input capacitance of up to 200pF with a faster discriminator.

VI. Acknowledgement

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VII. References

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