High-speed comparator IC with low time dispersion.

Atkin, E.V.

Moscow Engineering Physics Institute ,
Kashirskoe shosse 31, Moscow, Russia, 115409,
atkin@eldep.mephi.ru

Abstract

The high-speed comparator for fast time reference is presented. It can be used as a leading edge discriminator or as a core for building a constant fraction discriminator and can be useful for the development of time-of-flight systems.

It is manufactured with a bipolar process. Its main feature is a small dispersion of output signal time delay (200 ps) at a wide dynamic range of input signals (overdrives from 10 mV to 1V).

This paper describes the approach to the design of the new version of a low time dispersion comparator. The structure of such a comparator, features of schematics of its separate stages and its parameters are described.

I. INTRODUCTION

The incorporation of the necessary analog and digital processing units within a single chip is one of the ways to reduce the cost, dimensions and power consumption of contemporary read-out electronics. The paper reflects the results of the activities, being the continuation of the MEPhI group's efforts on developing precise timing discriminators [1, 2].

The most important and at the same time relatively expensive unit of a timing discriminator is, as a rule, the high-speed comparator. Therefore the next sections of the paper pay main attention to the aspects of development of the cost effective high-speed comparator IC for fast time reference.

This IC can be used as a leading edge discriminator or as a core for building constant fraction discriminator. It can be useful for the development of time-of-flight systems (such as ALICE TOF), providing a time reference accuracy at the order of tens of picoseconds.

II. THE APPROACH TO THE DESIGN

The analysis of literary sources has shown, that from the viewpoint of building the timing discriminator the most attractive high-speed comparator ICs are at present those from Analog Devices, Maxim and SPT. But unfortunately the mentioned ICs are not application specific ones.

Here there is presented the new version of a low time dispersion comparator. The structure of such a comparator and its schematics were designed to make it a functional analog (pin-compatibility as close as possible) of the well-known IC AD96685 from Analog Devices.

The designed IC is foreseen as an application specific one from the point of view the minimization of time dispersion of the propagation delay.

III. STRUCTURE AND SCHEMATICS

The comparator structure is shown in figure 1. Such a structure was chosen first of all in order to achieve the following goals concerning the characteristics of comparator:

- reduction of the dispersion of propagation delay;
- reduction of bias voltage;
- noise reduction;
- improvement of temperature stability.

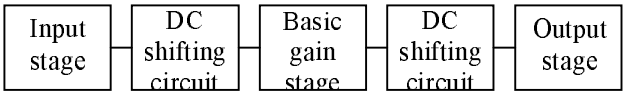

Figure 1: Comparator structure.

The comparator contains three symmetrical differential stages and is supplemented by the circuits of built-in hysteresis (from 0 to 4 mV) control and output signal logic variation. Its main peculiarity consists in the fact, that the small time dispersion of output signal (~200 ps) is specified for a wide dynamic range of input signals (overdrives from 10 mV to 1V) and for a temperature range from 0 to 70 °C. The propagation delays were determined with a 100 mV pulse.

The mentioned parameters were achieved at the expense of using:

- non-standard differential stages built as current amps;
- dynamic nonlinear loads, providing the compression of input signals.

Especial attention was paid to minimize the static errors and intrinsic noise of the comparator. The following table 1 presents certain comparator DC parameters.

Table 1: Comparator DC specifications

Parameter	**Value**	**Units**
Input bias current	20 max	μA
Input offset current	2.0 max	μA
Input offset voltage	2.0 max	mV
Input voltage range	±2.5	V
Intrinsic input noise	1.0 rms	mV

Outputs provide complementary digital signals fully compatible with the ECL 10K logic families. The output signal logic variation is provided by applying a control potential to a separate IC pin.

At designing the components of this comparator structure the following requirements were set to them.

To ensure the comparator operation in a wide dynamic range of signals with sufficiently low thresholds (~10 mV) the input stage must possess:

- small inherent noise and offset voltage, what implies the use of low-noise and well matched transistor pairs;
- small input currents (less than 10 μA), what limits the value of collector currents in the input stage at a specified β;
- sufficient amplification of signal (not less than 10) to ensure a good signal/noise ratio at the input of DC shifting circuit and a reduction of the following stage's influence on the noise and static parameters of comparator;
- capability to clip large amplitudes (above 1…2 V)

The basic gain stage should ensure an as great as possible amplification of signal (not less than 20) with a good temperature stability.

The output stage should provide a small voltage amplification of signal (not less than 5) and shape the specified logic step (GTL or ECL) across a typical capacitive load (units of pF). It also should provide a symmetrical swing of signals of both polarities.

Thus in total the gain of the three-stage comparator structure should amount to not less than 1000.

The DC level shifting circuits provide the matching of gain stages by bias and a partial compensation of their temperature instability.

A general requirement, set to all gain stages, is to minimize the dispersion of propagation delay for input signals of various amplitudes. Such a property of the stages is achieved by using non-linear techniques of signal processing. The basic idea of using non-linear circuits consists in the compensation with its help of the non-linearities of transistors, working in the circuit of a differential amplifier at the input of each stage, that is in the linearization of the comparator's transfer characteristic Uout (Uin).

In other words at a large dynamic range of input signals (more than 100) it is very important to provide the compression of signals by a factor of about 10 at the output of stage. In this case the following stages of the comparator will work in more comfortable conditions concerning the input signal range.

Finding the trade-off of signal amplification against propagation delay dispersion in each stage constitutes the basic problem of optimization. Here the traditional trend toward striving for a minimal propagation delay is abandoned and a choice is made in favour of reducing the dispersion of signal propagation delay.

The solution was found by using the following two circuital approaches:

- using differential circuits with non-linear dynamic loads;
- using such modes of transistor operation, at which particular comparator stages are drawn into saturation during the signal's rise-time, not entailing a considerable increase of signal delay.

IV. MAIN SIMULATION RESULTS

For the range of input overdriving signals from 10 mV to 1V the spread of propagation delay made up 200 ps in the temperature range from 0°C to 70°C. The typical dependences of propagation delay for the both transitions "1→0" (marked by ■) and "0→1" (marked by ◊) are shown in figure 2.

Power consumption amounted to 180 mW at supply voltages ±5V. The absolute value of propagation delay did not exceed 5 ns at overdrive voltages more than 10 mV and pulse amplitude of 100 mV.

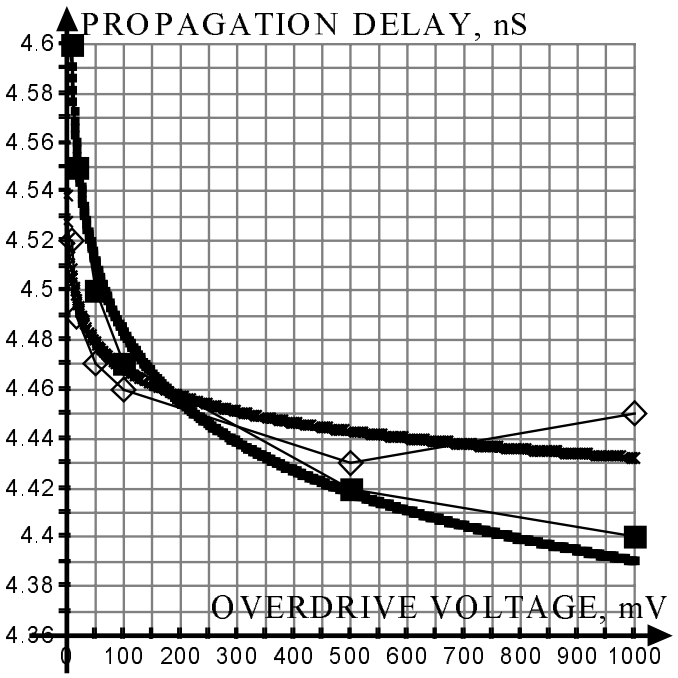

Figure 2: Typical dependences of propagation delay.

V. REFINEMENT OF MODELS

The mentioned comparator versions were designed on the basis of an application specific semicustom array (ASSA), manufactured by bipolar technology with $f_t \geq 5$ GHz [3].

In order to obtain more reliable simulation results there were refined the SPICE-models of certain ASSA components. Particularly, that were the temperature coefficients of the base-emitter junctions, Zener diodes and the different types of resistors. The spread of Zener breakdown voltages and noise of Zener diodes was studied as a function of bias current.

By using the refined models there were verified the static, dynamic and noise characteristics of ASSA components. The measured parameters are partially adduced in table 2. There are presented measurement results for samplings of 20 transistors and resistors.

Table 2: Typical spread of ASSA component parameters

Parameter	ΔI_1 (10…600 μA)	ΔI_2 (600…1000 μA)	ΔI_3 (1..1,6 mA)	ΔT_1 (20..70°C)	ΔT_2 (70..130°C)
$\Delta U_{be\ 2x6}$, mV	322	21	40	-80 (I=820μA)	-73 (I=820μA)
$\Delta U_{be\ isogr}$, mV	0,5	5	30	–	–
$\Delta U_{be\ 2x18}$, mV	38	25	96	–	–
ΔU_{ZEN}, V	0,85	0,18	0,14	0,05 (I=600μA)	0,06 (I=820μA)
ΔR_{HR}, kOhm	–	–	–	0,48 (12%)	0,39 (9%)
ΔR_{LR}, Ohm	–	–	–	-32 (6%)	6 (1%)

In the first column there are enumerated the following parameters:

$\Delta U_{be\ 2x6}$ – spread of base-emitter voltage of transistors, having the emitter strip size of 2x6 μm sq.;

$\Delta U_{be\ isogr}$ – spread of base-emitter voltage of the isogradient transistor pair;

$\Delta U_{be\ 2x18}$– spread of base-emitter voltage of transistors, having the emitter strip size of 2x18 μm sq.;

ΔU_{ZEN} – spread of the stabilization voltage of Zener diodes;

ΔR_{HR} – spread of resistance of high-ohmic resistors;

ΔR_{LR} – spread of resistance of low-ohmic resistors.

The second, third and fourth columns contain the results of measuring the spread of parameters (in a batch of samples) in three sub-ranges of working currents.

The fifth and sixth columns present the change of parameters for two temperature ranges at fixed bias currents.

It follows from the table data, that a partial temperature compensation of the Zener diode's change in breakdown voltage is possible by means of the base-emitter junction of a transistor, connected in a follower circuit. It is also apparent, that the temperature coefficients of low-ohmic and high-ohmic resistors in the temperature range of (0…70)°C have values of opposite sign and close modulus and therefore can be employed to create thermo-stable potentials. Besides that, the data, presented in table 1, allow to make a conclusion on the optimality of transistor currents in the range of (600…1000) μA and Zener diode currents in the range of (600…1600) μA.

VI. COMPARISON WITH ANALOGS

Table 3 presents the typical basic parameters of the designed comparator and several well-known foreign functional analogs, having a small dispersion of propagation delay.

Table 3: Comparison of the designed comparator with analogs.

№	Parameter	AD96687	MAX 911	MEPhI comparator	Unit of measurement
1.	**Offset voltage**	1[1)]	1	0,5[2)]	mV
2.	**Input current**	7	3	8	μA
3.	**Gain**	~ 60	~ 60	~ 60	dB
4.	**Propagation delay**	2,5	4	4,5	ns
5.	**Dispersion of propagation delay**	50[3)]	500[4)]	200[5)]	ps
6.	**Output logics**	ECL	ECL	ECL, GTL[6)]	-
7.	**Power consumption**	120	200	180	mW

Remarks:

1) At a source resistance of 100 Ohm

2) At a source resistance of 50 Ohm

3) At overdrives from 100 mV to 1V

4) At overdrives from 10 mV to 100 mV and an input rise-time of 500 ps.

5) At overdrives from 10 mV to 1 V and an input rise-time of 100 ps

6) Is selected by the choice of supply voltage.

Analyzing the data of table 3 one can conclude, that the designed comparator in comparison with the other ones presented has a small dispersion of propagation delay at a comparable power consumption and a larger absolute propagation delay. Let us note that the latter is not principal for building fast time reference units.

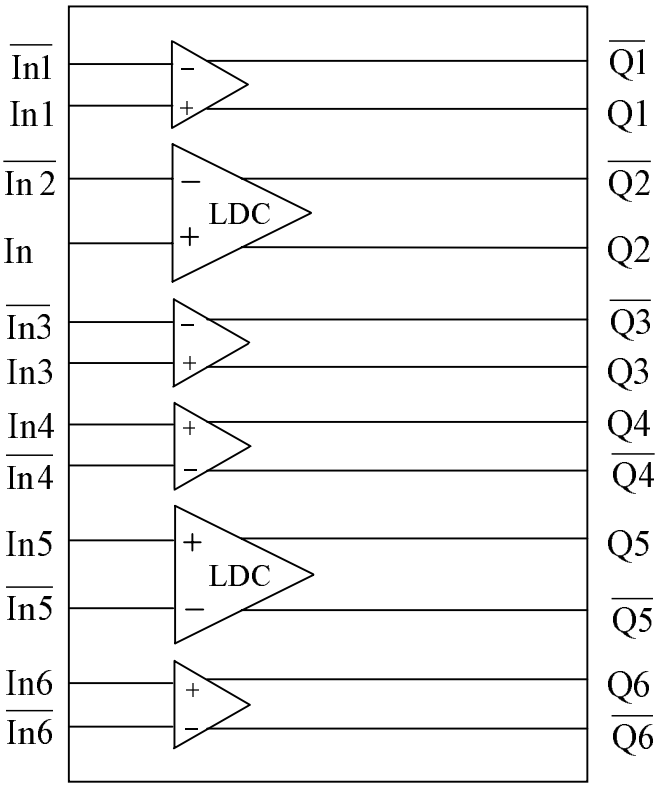

Figure 3: IC contents and partial pin assignment

VII. ENCAPSULATION

The designed comparator is encapsulated as a two-channel variant in a single package together with additional four micropower comparators, built according to standard circuit schematics. A partial pin assignment is presented in figure 3.

The given disposition of pins implies the possibility to replace standard well-known comparators (AD96687, MAX9687 and so on).

The joint encapsulation of two low dispersion comparators in a single package with four micropower comparators allows to create with only one IC package a double channel timing discriminator according to the structural diagram of one channel, presented in figure 4.

In this diagram one micropower leading edge comparator (LED1) operates in the mode of switching by the input leading edge at a specified threshold voltage. The second micropower comparator (LED2) is responsible for shaping the output signal from the ones of the comparator with low dispersion of propagation delay (LDC), operating in the constant fraction mode, and of the first micropower comparator.

At the bottom of figure 4 there is a linear axis which shows the typical propagation delay scale inside each channel of the timing discriminator structure.

VIII. FIRST APPLICATION

The given IC was designed in the limits of an International Science and Technology Center (ISTC) project. The first probation of the designed comparators is expected to take place in the channels, collecting the signals of avalanche detectors of the self-quenching Geiger counter type [4].

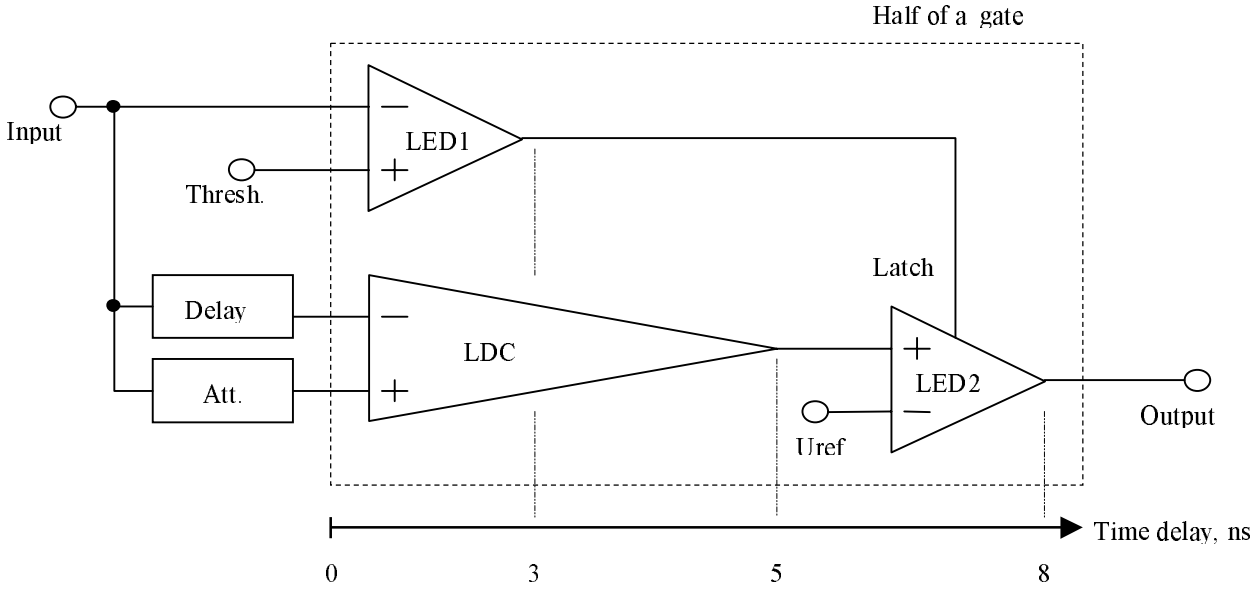

Figure 4: Structural diagram of one channel

In the nearest future it is planned to design the prototype SMT boards of a timing CFD based on the manufactured ICs. It is expected that the time reference accuracy will reach the value of about 50 ps at the range of input signals from 10 mV to 1000 mV.

IX. Conclusions

The high-speed comparator for fast time reference was designed and manufactured in a bipolar process. Its main feature is a small dispersion of the output signal`s delay (200 ps) at a wide dynamic range of input signals (overdrives from 10 mV to 1V).

X. References

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