

# Measurements of Radiation Effects on the Timing, Trigger and Control Receiver (TTCrx) ASIC

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## *Abstract*

The Timing, Trigger and Control Receiver ASIC (TTCrx) receives and distributes the clock, the trigger decision, and other synchronisation signals. In this paper, the effects of radiation on the chip, manufactured in the 0.8  $\mu\text{m}$  BiCMOS DMILL technology, are discussed. The paper is divided into three sections: In the first part, the architecture of the circuit is described, where we concentrate on the measures taken to increase robustness with respect to single event upset (SEU) effects. In the second part, we will present measurements of the circuit characteristics before and after irradiation with gammas and neutrons. In the third part, we will then show measurements of single event effects.

## I. INTRODUCTION

In the Timing, Trigger and Control (TTC) system [1], the LHC clock is transmitted together with the first level trigger and control information over optical fibers using a bi-phase mark encoding scheme. At the receiver side, the signal is detected by a PIN-photodiode and fed into the TTC receiver (TTCrx) ASIC, where clock and data are extracted and made available to the connected detector electronics. If the circuit is deployed in a radiation environment two groups of effects, i.e. long-term cumulative effects on the one hand, and single-event effects (SEEs) on the other hand, have to be investigated. While cumulative effects have an influence on the analog performance parameters of the circuit (in the case of the TTCrx: clock jitter and clock deskewing linearity), SEEs lead to a momentary malfunction of the device.

## II. ARCHITECTURE

A block diagram of the TTCrx IC is shown in Fig. 1. In the Limiting Amplifier (LA), the signal from the PIN-diode is amplified and converted to CMOS levels. An internal phase-locked loop (PLL) then recovers the clock and the serial data stream, which is then demultiplexed into two 40 Mbit/s channels, denoted A and B. While channel A is reserved for the trigger signal, channel B contains data in the form of broadcast commands and individually addressed commands. The original clock signal goes into two independent clock deskewing units, where the clock phase can be selected with programmable delay. The configuration and control registers, the counters, and the status register are linked together via an internal bus, which can be accessed via an I<sup>2</sup>C interface [2].

## III. DESIGN MEASURES AGAINST SEU

In order to achieve robustness against single event upsets (SEUs) several design measures were taken. The major difficulty proved to be

the limitation that the given package did not allow a die size bigger than 5.2x5.2 mm. Hence the chip area was very limited, forbidding extensive measures such as the introduction of triple redundancy in all state machines. Regarding these limitations, the goal was defined that the TTCrx should, on the long term, maintain operation without any system interaction. It was therefore found crucial to protect the configuration registers, since they contain vital data such as the values of the bias currents, the identification number, and the mode of operation of the circuit.

As seen in Fig. 1, an SEU correction check machine is connected to the registers via the internal bus. Every byte in the configuration register is protected with four Hamming check bits. The error correction machine cyclically monitors the registers, and corrects it within 1ms in case that an SEU has occurred. An SEU counter is increased when a bit was corrected. This counter can be interrogated via the I<sup>2</sup>C bus.

In order to avoid that the chip gets stuck in an undefined state, a watchdog circuit was added, which monitors the correct operation of the circuit. If the PLL should lose lock for more than 50ms, an automatic reset is performed. While the configuration registers are then loaded with default values, the register content of the control register and the fine and coarse deskewing registers remain unchanged.

## IV. CUMULATIVE EFFECTS DUE TO GAMMA AND NEUTRON IRRADIATION

The following tests were made to assess the influence of neutron and gamma irradiation on two important analog parameters: clock jitter and clock deskewing linearity.

### A. Clock jitter

The chip was irradiated with a 10 keV gamma source, and long-term jitter with respect to the clock reference of the TTC transmitter crate was measured as a function of the optical input power. The data sent on the link was either the 0-1 idle pattern, or, in the second case, random data in channel B combined with triggers with a 220 kHz rate in channel A. All measurements were performed using a PGA package for the TTCrx and a Honeywell/Lytel HFD 8005 photodiode.

The results can be seen in Fig. 2 (rms jitter) and Fig. 3 (peak-to-peak jitter). The black curves show the pre-rad situation, where the solid line corresponds to the idle pattern and the dotted line to random data. The gray curves show the situation after an 8 Mrad gamma irradiation. It is remarkable that in the case of the idle pattern the irradiated chip shows lower jitter for nearly the entire range of optical input power. When random data is transmitted, the irradiated chip shows better performance for high levels of optical input power, whereas jitter is higher for smaller power levels. To explain these

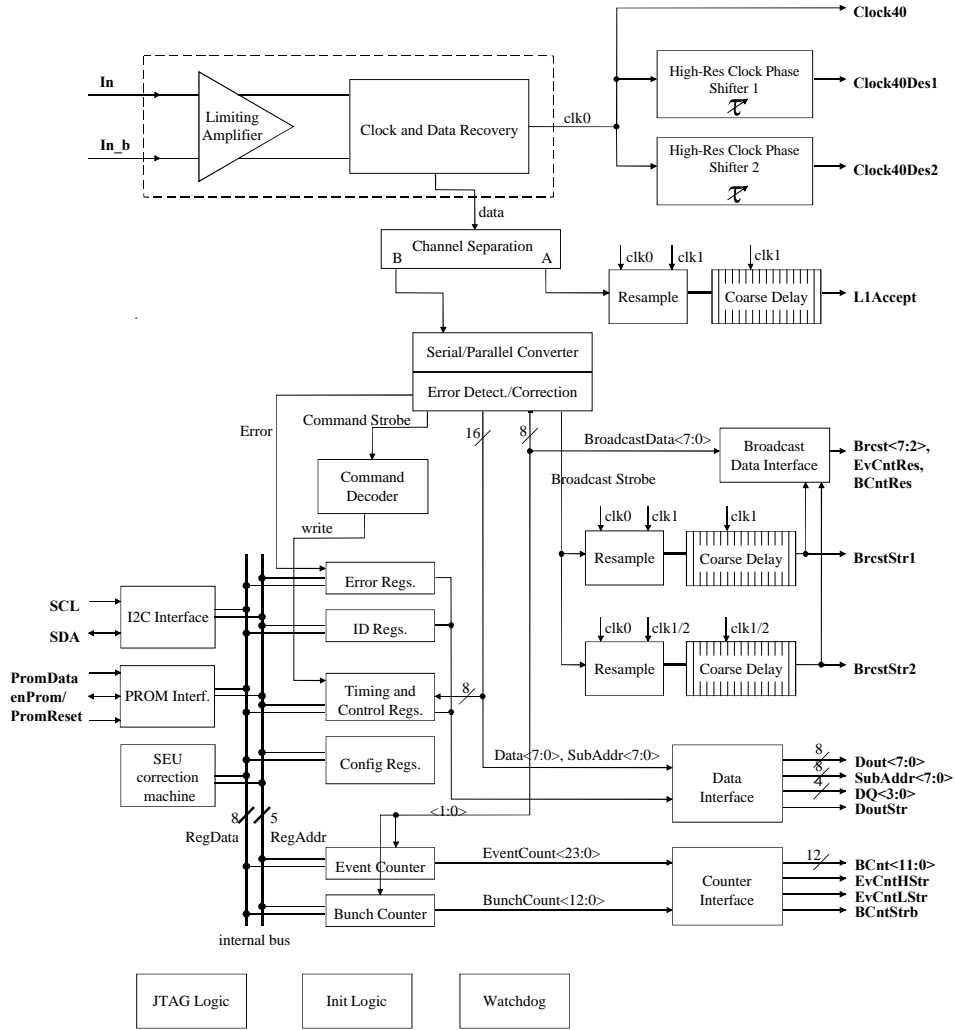


Figure 1: Block diagram of the TTCrx ASIC.

Figures 4 and 5 display the corresponding measurements for the case of a  $5 \times 10^{13}$  neutrons/cm<sup>2</sup> irradiation, showing a similar behavior.

results, the signal flow from the photodiode to the PLL in the TTCrx chip, shown in Fig. 6, has to be considered: Both, the pre-amplifier integrated with the photodiode and the on-chip Limiting Amplifier (LA), can be modeled as a low-pass filter, having a certain gain and cut-off frequency. The signal is AC-coupled via coupling capacitor  $C_{\text{coupl}}$ , thereby forming a high-pass filter together with the input resistance  $R_{\text{in}}$  of the LA. A (sinusoidal) signal going through any filter experiences a frequency-dependent delay

$$\Delta t = \frac{\varphi(\omega)}{\omega},$$

with  $\varphi(\omega)$  denoting the phase response of the filter as a function of frequency. In a simplified model, the incoming biphas encoded bitstream contains either 40 MHz or 80 MHz components. (This corresponds to a steady bitstream of either only zeroes or only ones.) The high-pass filter acts as a pre-emphasis filter and partially equalizes the signal delay difference stemming from the low-pass filter. By choosing the coupling capacitance, the jitter behavior can be optimized.

The time constants of both the low-pass filter and the high-pass filter change with irradiation, in the former case, caused by a decrease in bandwidth due to the degradation of the bipolar  $\beta$ , in the latter case due to the change in the input resistance of the LA, thereby shifting the pole of the HPF.

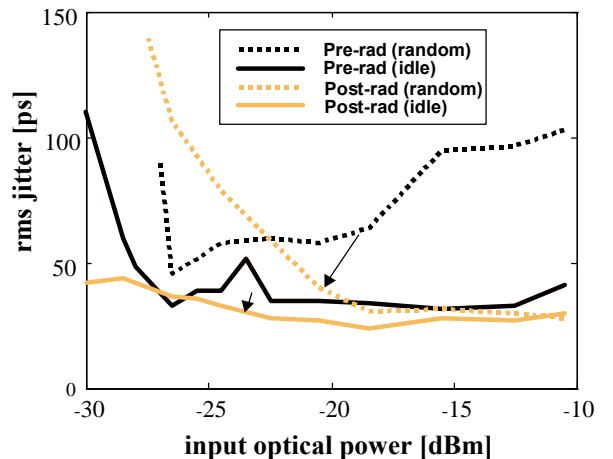


Figure 2: RMS clock jitter as a function of optical input power, in the pre-rad case and after a 8 Mrad gamma irradiation.

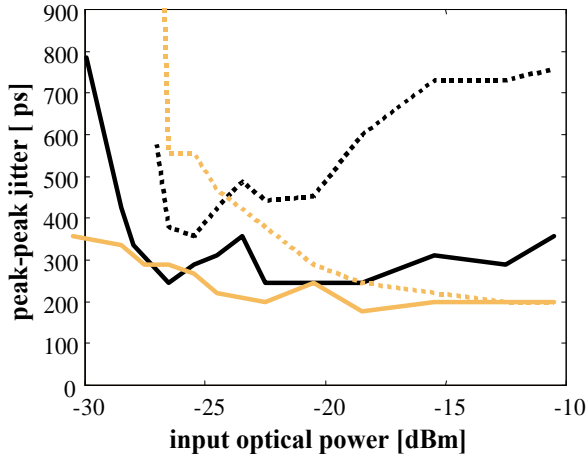


Figure 3: Peak-to-peak clock jitter as a function of optical input power, in the pre-rad case and after a 8 Mrad gamma irradiation.

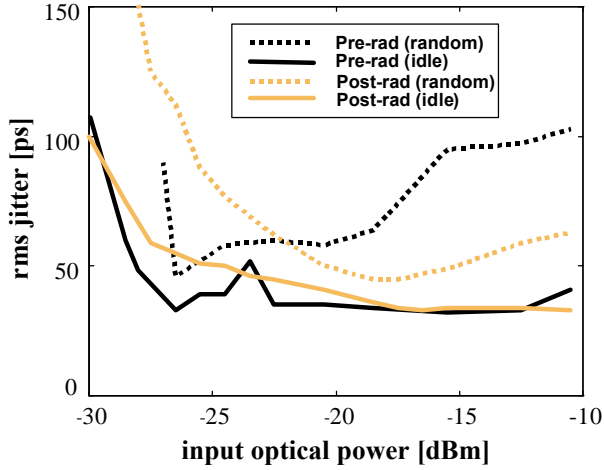


Figure 4: RMS clock jitter as a function of optical input power, in the pre-rad case and after neutron irradiation.

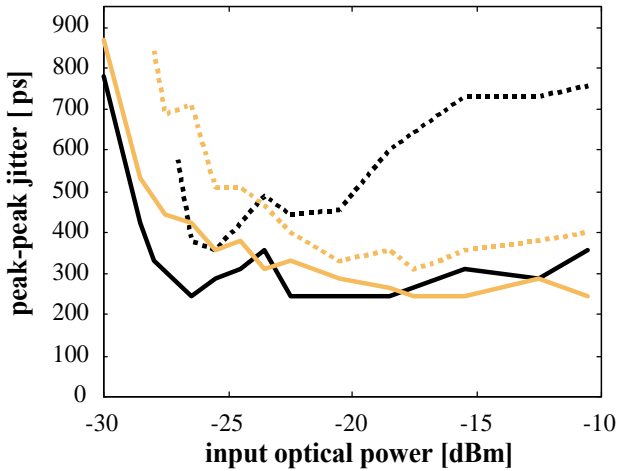


Figure 5: Peak-peak clock jitter as a function of optical input power, in the pre-rad case and after neutron irradiation.

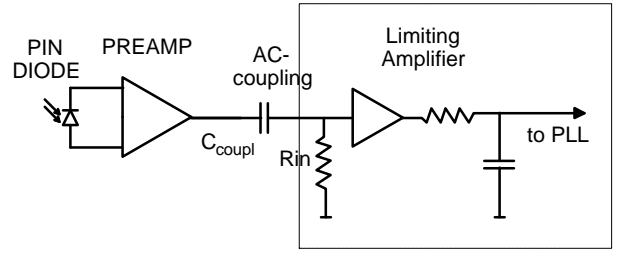


Figure 6: Input signal path. Both the preamp and the Limiting Amplifier can be modeled as a low-pass filter. The coupling capacitance together with the input impedance forms a high-pass filter.

### B. Clock deskewing linearity

The influence of irradiation on the clock deskewing non-linearity is shown in Figures 7 and 8 (close-up view). It can be verified that the non-linearity does not substantially degrade after gamma irradiation, and gets slightly better after neutron irradiation. The results are summarized in Table 1.

Table 1: Clock Deskewing non-linearity.

Condition	Differential NL		Integral NL	
	$\sigma$ [ps]	p-p [ps]	$\sigma$ [ps]	p-p [ps]
Pre-rad	48	324	74	326
Gamma	75	425	95	364
Neutrons	36	190	70	357

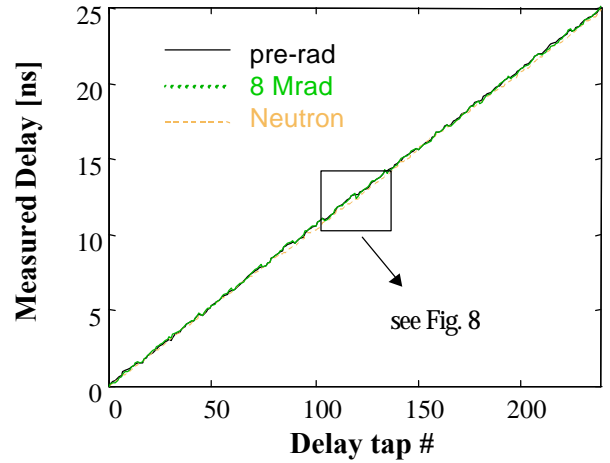


Figure 7: Clock skewing non-linearity. The graph shows the measured delay as a function of programmed delay tap.

## V. SINGLE EVENT EFFECTS

To investigate SEU effects, the chip and the photodiode were irradiated with heavy ions, protons and neutrons at the Cyclone facility at Louvain-la-Neuve, Belgium. The operation of the circuit was continuously monitored by reading the whole register file via the I2C port, and logging whenever a register content changed due to an SEU.

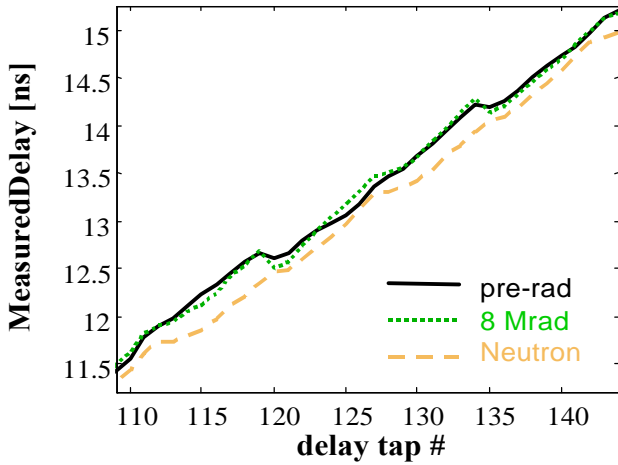


Figure 8: Deskewing non-linearity. Magnified graph showing the measured delay as a function of programmed delay.

Getting sufficient statistics for SEU measurements is difficult in a custom chip, since not all SEUs can be easily detected, as is the case in a dedicated SEU test chip which e.g. contains a long shift register. In the TTCrx, the register file proved to be a useful source for statistics. There are 10 eight bit registers, each having a 4 bit wide Hamming check code, resulting in a total of 120 Flip-flops. Any change in one of those registers was detected and corrected by the Hamming error correction machine, thereby incrementing the SEU counter. Most SEUs in the SEU counter itself were detected by noting that the counter value changed by a value of  $2^n$  ( $n \geq 1$ ). In addition, the 24 bits of the event counter were monitored for SEUs.

#### A. SEU Cross section as function of particle LET

The chip was irradiated with various heavy ions of different LET. Figure 9 shows the derived cross-section as a function of LET of a DMILL flip-flop. Fitting a Weibull curve results in a threshold LET of at least  $7.5 \text{ MeV cm}^2/\text{mg}$ . This value is however pessimistic, because due to the small number of registers accessible, the statistics around  $\text{LET}_{th}$  is sparse.

#### B. On-Chip Single Event Effects due to Protons and Neutrons

The chip was irradiated with  $10^{11}$  protons of an energy of 60 MeV. While powering the chip with a supply voltage of 5.0 V, no error was detected. At a supply voltage of 3.3 V, the chip lost lock once. Assuming a threshold LET of  $7.5 \text{ MeV cm}^2/\text{mg}$ , a total fluence of  $10^{14}$  60 MeV protons/cm<sup>2</sup> (which corresponds to the fluence found e.g. in the ATLAS silicon tracker disk part), and a security factor of 10 leads to the numbers of particular errors for one device listed in Table 2.

When irradiating the chip with  $1.2 \times 10^{10}$  neutrons/cm<sup>2</sup> with an energy of 60 MeV, no SEU was noticed.

#### C. Single Event Effects due to irradiation of the photodiode with Protons and Neutrons

In a second experiment, a proton beam was directed on the PIN-photodiode. All measurements were done using a HFD 8005 Lytel diode packaged by Honeywell, and an optical signal with  $-21 \text{ dBm}$

input power. The result was that, due to the particles traversing the photo diode, the chip loses lock with a probability depending on the incident angle of the beam and the input power of the optical signal. This can be explained by direct ionization, as described in detail in Ref. [4]. The charge which is generated by ionizing particles in the photodiode causes an electrical current which adds to the signal produced by electron-hole generation due to photons. The PLL in the TTCrx requires the signal edges to occur within a  $\pm 3.125 \text{ ns}$  window [3]. If a traversing particle generates enough charge on the diode, the signal edge in the original signal can be hidden, which eventually leads to a loss of lock in the PLL.

Table 2: Estimated number of SEU events for a total fluence of  $10^{14}$  60 MeV protons/cm<sup>2</sup> and a security factor of 10.

Error description	Total events
Configuration register (corrected)	87
Event counter	14
Bunch counter	7
PLL loses lock	35
Double bit Transmission errors	6
False triggers	7
I2C interface lost	1

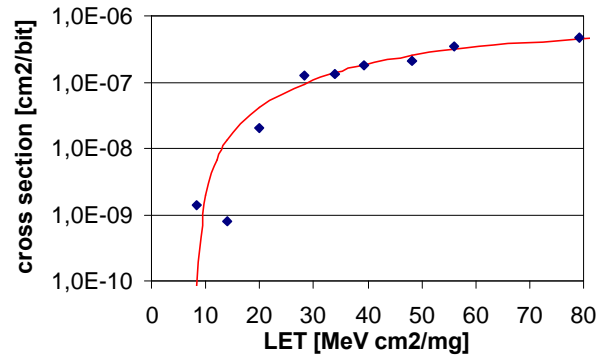


Figure 9: Cross section of a DMILL flip-flop as a function of LET.

The cross section for the "loss of lock" event for various conditions is shown in Figure 10. The three leftmost bars correspond to the case of a 60 MeV proton irradiation showing different incident angles of the beam. The maximum occurs at an angle of 0 degrees with the diode surface, in which case the protons arrive in the direction of the p-n junction. With 30 MeV protons and an angle of 0 degrees, no single event effect was seen. This can be explained by the shielding effect of the metal package.

The rightmost bar shows the result for the case of a neutron beam at an angle of 0 degrees. It was verified in [4] that, unlike the proton case, the upset rate does not show any angle dependency for neutrons, due to the absence of direct ionization. Assuming a total fluence of neutrons with an energy  $> 20 \text{ MeV}$  of  $10^{13}/\text{cm}^2$ , and an LHC beam time of

$10^8$  s, this corresponds to one loss of lock event every 6000 seconds, and a false trigger at every 50000 seconds, which was considered to be too high. The measurements in [4] suggest that increasing the optical input power by 6 dB reduces these rates by a factor of 10. The design was however modified in order to make the chip less susceptible to this problem: The PLL of the TTCrx now tolerates that an isolated edge of the input signal is missing. The chip with this modification was submitted to fabrication in July 2000.

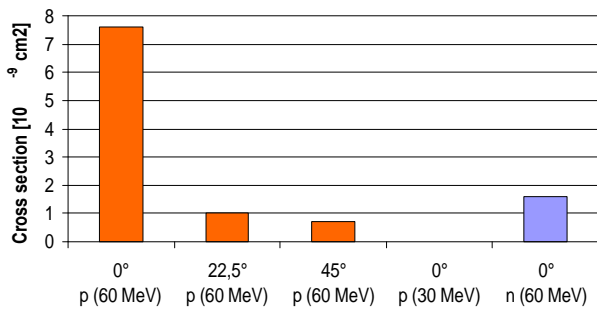


Figure 10: Cross section of "loss of lock" event for proton and neutron irradiation for different energies and angle.

## VI. CONCLUSIONS

In this paper we characterized the TTCrx with respect to both cumulative and single event radiation effects. It was shown that cumulative effects change the jitter characteristics of the circuit due to a change in the frequency response of the system.

Clock deskewing linearity was affected by both gamma and neutron beams, where the former lead to a slight decrease in performance, the latter to a slight improvement. The degradation was however within reasonable bounds.

Concerning single event effects it was shown that the chip itself is rather insensitive to SEUs. In addition, the Hamming check machine successfully corrects occurring errors in the configuration registers, such that they do not change their value for a long time. It must however be taken into account that during a period of about 1ms these values can be wrong (e.g. the clock fine deskewing parameters).

It was found that the biggest problem came from single event effects on the photodiode making the chip lose lock. A fix for this problem was incorporated into the final chip design.

## VII. ACKNOWLEDGMENTS

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## VIII. REFERENCES

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